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METHOD AND APPARATUS FOR DETERMINING A PROCESSING SPEED OF AN INTEGRATED CIRCUIT

INVENTOR:

Greg Sadowski
321 Harvard Street
Apt. 303
Cambridge, MA 02139

ASSIGNEE:

ATI Technologies, Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada L3T 7X6

ATTORNEY OF RECORD:
TIMOTHY J. BECHEN
REGISTRATION NO. 48,126
VEDDER, PRICE, KAUFMAN & KAMMHOLZ, P.C.
222 NORTH LASALLE STREET, SUITE 2600
CHICAGO, ILLINOIS 60601
PHONE (312) 609-7500
FAX (312) 609-5005

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Name of Depositor: Karenina Oliver

Signature: Karenina Oliver

METHOD AND APPARATUS FOR DETERMINING A PROCESSING SPEED OF AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuits and more specifically to determining a processing speed of the integrated circuit.

BACKGROUND OF THE INVENTION

[0002] An application specific integrated circuit (ASIC) is typically generated on a silicon wafer having a plurality of etchings for transmitting electrical signals and other chemical elements, such as Gallium Arsenide etched thereon for providing electrical functionality, such as transistors. In a typical assembly process, a plurality of integrated circuits are formed on a single wafer and portions of the wafer are tested to determine temperature, supply voltage and process variations. In a typical system, process variations are measured once during the production test of the ASIC and a speed grade is assigned to the individual integrated circuits. The temperature is measured in the system in which the integrated circuit is operating and the result is, in some designs, used for controlling a clock frequency. Moreover, voltage can be measured and the results used, by some designs, to control clock frequency.

[0003] The above-noted solutions treat the process variations, supply voltage and temperature measurements separately, and thereupon try to combine them on a system level. This solution may not lead to an optimal characterization of the performance characteristics of a specific integrated circuit due to relative intrinsic values, such as temperature dependency of multiple integrated circuits based on the number of process variations and differences in supply voltages.

[0004] Furthermore, when a plurality of integrated circuits are generated on a single wafer, the division of the individual integrated circuits from the wafer is typically performed by a cutting process. A binning operation is performed, wherein integrated circuits having specific performance levels are provided to specific corresponding bins. For example, if a fabricated wafer containing a plurality of integrated circuits contains integrated circuits having performance speeds within ten different ranges, the binning process consists of sorting and disbursing the integrated circuits into ten separate categories. The above-noted prior art performance determination process does not allow for binning of the specific integrated circuits, based on general testing and due to the reduction in the amount of die space in current fabricated integrated circuits.

[0005] As such, there exists a need for a method and apparatus that allows for determining a processing speed of an integrated circuit, wherein the integrated circuit may be on a wafer having a plurality of integrated circuits, wherein the performance speed is determined independent of process, voltage and temperature measurements and may be based on the execution of a system application on the integrated circuit. Moreover, there also exists a need for determination of processing speeds for integrated circuits of the plurality of integrated circuits to improve the binning process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 illustrates an apparatus for determining a processing speed of an integrated circuit in accordance with one embodiment of the present invention;

[0007] FIG. 2 illustrates a schematic block diagram of an apparatus for determining a processing speed of an integrated circuit in accordance with another embodiment of the present invention;

[0008] FIG. 3 illustrates a schematic block diagram of an alternative embodiment of an apparatus for determining a processing speed of an integrated circuit;

[0009] FIG. 4 illustrates a timing diagram representing timing signals generated by the apparatus for determining the processing speed of an integrated circuit;

[00010] FIG. 5 illustrates a flow chart of a method for determining a processing speed of an integrated circuit;

[00011] FIG. 6 illustrates a flow chart of an alternative method for determining the processing speed of an integrated circuit in accordance with one embodiment of the present invention;

[00012] FIG. 7 illustrates a method for determining the processing speed of an integrated circuit and performing a binning operation thereon, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[00013] Generally, a method and apparatus for determining a processing speed of an integrated circuit includes a first flip flop, such as a D flip flop, having an input port capable of receiving an input signal. The input signal may be any type of data signal, such as a pseudo-random generated signal. The first flip flop also has an output port which is capable of providing a flip flop output signal, in accordance with known flip flop technology, and a timing port

capable of receiving an incoming clock signal. The incoming clock signal may be a timing signal having any suitable clock frequency for determining the processing speed of the integrated circuit.

[00014] The method and apparatus further includes a delay circuit operably coupled to the output port of the first flip flop, such that the delay circuit is capable of receiving the flip flop output signal and generating a delayed timing signal. The delay circuit includes one or more delay buffers and a plurality of gates which provide for a delay of the incoming flip flop output signal. The delay timing signal furthermore may be a time offset timing signal. The method and apparatus further includes at least one clock speed adjusting circuit operably coupled to the delay circuit. Similar to the delay circuit, the clock speed adjusting circuits include delay buffers and various combinations of gates to provide for a specific timing offset.

[00015] The method and apparatus further includes a multiplexer operably coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the multiplexer further has a selective delay input port capable of receiving a select delay signal. The select delay signal may be a signal indicating which one of the clock speed adjusting circuits, if any, are to be chosen by the multiplexer as an output signal. Moreover, the multiplexer receives output signals generated by the clock speed adjusting circuits and the delay timing signal wherein the output signal generated by the delay timing signal is indicative of the lack of a clock speed adjusting circuit between the delay circuit and the multiplexer. Based on the select delay signal, a multiplexer output signal is chosen and provided to an input port of a second flip flop. In one embodiment, the second flip flop may be a D flip flop. The second flip flop further includes an output port capable of providing a timing output signal and a timing port capable of receiving the

incoming clock signal. Therein, based upon a comparison of the timing output signal relative to a control timing signal, the processing speed of the integrated circuit may be determined.

[00016] More specifically, FIG. 1 illustrates an apparatus 100 for determining a processing speed of an integrated circuit 102, the apparatus 102 may also be disclosed as a speed sensor. As recognized by one having ordinary skill in the art, the apparatus 100 may be disposed within a die on an ASIC, wherein the apparatus 100 can determine performance characteristics relative to the corresponding ASIC circuit upon which the apparatus 100 is disposed thereon. The apparatus 100 includes a first flip flop 104, such as a D flip flop, capable of receiving an input signal 106 in an input port 108. The first flip flop 104 also receives a clock signal 110 in a timing port 112 and generates a flip flop output signal 114 provided via an output port 116. The apparatus also includes a delay circuit 120 capable of receiving the flip flop output signal 114 and therein generating a delayed timing signal 122, in accordance with known delay circuit technology.

[00017] The delay timing signal 122 is provided to a plurality of clock speed adjusting circuits, 124, 126, 128 and 130. The clock speed adjusting circuits, similar to the delay circuit 120, include delay buffers in various combinations of gates to provide for a specific clock signal delay. Moreover, the clock speed adjusting circuits 124, 126, 128 and 130 are illustrated in FIG. 1 as representing 105%, 110%, 115% and 120%, respectively. As recognized by one having ordinary skill in the art, these percentages are exemplary only and any other suitable offset delay may be provided by a correspondingly generated clock speed adjusting circuit.

[00018] A multiplexer 132 receives output signals 134, 136, 138 and 140 from the clock speed adjusting circuits and, in one embodiment, receives the delay timing signal 122 provided

from the delay circuit 120. The multiplexer 132 further receives a select delay signal 142, wherein the select delay signal indicates which one of the delays, such as no delay at 100%, 105%, 110%, 115% or 120%, of the delay timing signal 122 is to be chosen as a multiplexer output signal 144. Therefore, in response to the select delay signal 142, the multiplexer 132 provides the multiplexer output signal 144 to a second flip flop 146, such as a D flip flop. An input port 148 of the second flip flop receives the multiplexer output signal 144, a timing port 150 of the second flip flop receives the incoming clock signal 110 and, in accordance with known flip flop technology, a timing output signal 152 is generated and provided via an output port 154 of the second flip flop.

[00019] Therefore, based on the timing output signal 152, a determination of the processing speed of the apparatus 100 may be determined wherein the processing speed is indicative of the processing speed of the integrated circuit 102, having the apparatus 100 sensor, disposed therein.

[00020] FIG. 2 illustrates an alternative embodiment of an apparatus for determining the processing speed of the integrated circuit 102, using a 3 flip flop module 200, otherwise referred to as a 3 flop module. Similar to the apparatus 100, the input signal 106 is provided to the first flip flop 104, wherein the first flip flop 104 provides the flip flop output signal 114 to a first delay module 202. The first delay module is further coupled to the second delay module 204, wherein the first delay module 202 and the second delay module 204 both receive the select delay signal 142 and the incoming clock signal 110.

[00021] The first delay module 202 contains elements similar to the apparatus 100 excluding the first flip flop 104. Both the first delay module 202 and the second delay module

204 include a delay circuit 120A and 120B, a multiplexer 132A and 132B, the first delay module 202 includes the second flip flop 146 to receive the multiplexer output signal 144A and the second delay module 204 includes a third flip flop 206 to receive the multiplexer 132B multiplexer output signal 144B.

[00022] The utilization of 3 flip flops, 104, 146 and 206, provides redundancy in the utilization of the delay modules 202 and 204 and provides for the timing output signal 152 to be more reliable when compared to a control clock signal, not specifically illustrated. The second delay module 204 receives an interim timing signal 208 from the first delay module 202, wherein the interim timing output signal 208 is similar to the timing output signal 152 containing a timed offset signal.

[00023] As recognized by one having ordinary skill in the art, the clock speed adjusting circuits 124, 126, 128 and 130 illustrated within the first delay module 202 and second delay module 204, are for exemplary purposes only and any other suitable clock speed adjusting circuit having a different clock speed adjusting value may be utilized therein.

[00024] FIG. 3 illustrates another embodiment of an apparatus for determining a processing speed of an integrated circuit, including the three flop module, apparatus 200 of FIG. 2. The three flop module 200 receives the input signal 106 from a pseudo-random generator 302. The pseudo-random generator may be any type of input signal generation device or module such that a pseudo-random input signal 106 may be generated. The three flop module 200 further receives the select delay signal 142 from a sequencer 304. In one embodiment, the sequencer 304 may be a device or module capable of selecting different clock speed adjusting circuits to be chosen by the multiplexers 132 within the three flop module 200. In this embodiment, the

sequencer 304 generates a plurality of select delay signals which may be used for repetitive and reiteration of selecting multiple timing sequences for being tested to determine the processing speed of the integrated circuit.

[00025] Further included within the apparatus 300 are a plurality of control timing flip flops 306, 308 and 310. The first of the control timing flip flops 306 receives the input signal 106 from the pseudo-random generator 302, provides an output signal 312 to the second flip flop 308 of the control timing flip flop and a second output signal 314 is provided to the third flip flop 310 of the control timing flip flops. In one embodiment, the three controlled timing flip flops 306, 308 and 310 are D flip flops which mirror the flip flops 104, 146 and 206 within the three flop module 200. The third flip flop 310 of the control timing flip flops generates a control timing signal 316, which is provided to a logic gate 318.

[00026] Control timing flip flops 306, 308 and 310 also receive the incoming clock signal 110, which is provided to the three flop module 200. The incoming clock signal 110 may be provided from any suitable clock sources recognized by one having ordinary skill in the art.

[00027] The logic gate 318 receives the control timing signal 316 and the timing output signal 152. In one embodiment, the logic gate 318 is an XOR gate for comparing the exclusive OR arrangement of the timing output signal 152 relative to the control timing signal 316.

[00028] The apparatus 300 further includes a register 320 operably coupled to receive the delay select signal 142 from the sequencer 304 and the incoming clock signal 110. Disposed between the register 320 and the logic gate 318 is a logic gate flip flop 322, such as a D flip flop. The logic gate flip flop 322 receives the incoming clock signal 110 and timing indicator signal 324 from the logic gate 318

[00029] The logic gate flip flop 322 thereupon generates a timing result signal 326 which may be a signal indicating if the three flop module 200 was able to process the input signal 106 from the pseudo-random generator 302 at the speed designated by the delay timing signal 142. The register 320 receives the timing results signal 326 and storage this indicator therein.

[00030] In one embodiment, the above processes repeated using another pseudo-random generated input signal 106 and another select delay signal 142 from the sequencer 304. The processes repeated until the register 320 contains enough timing result signals 326 to make an accurate determination of the processing speed of the integrated circuit.

[00031] As recognized by one have ordinary skill in the art, logic gate 318 is illustrated here and as a XOR gate, but maybe any other suitable combination of logic gates provided for the indicator 324 which is provided to the logic gate flip flop 322.

[00032] FIG. 4 illustrates a timing diagram representing a clock signal 110 having a clock interval 402 relative to the timing sequence of multiple signals. The second timing signal represents the flip flop output signal 114 provided from the first flip flop 104 illustrated in FIG. 1. The other five timing signals represent timing transitions of the delay timing signal 122 and clock adjusted signal 134, 136, 138 and 140, as illustrated in FIG. 1 from the polarity of clocks speed adjusting circuits 124, 126, 128 and 130 respectively.

[00033] As illustrated herein, a setup time 404 indicates the transition of the incoming timing signal 110 from a low state to a high state as compared to the corresponding timing signals 122 and 134-40. In the exemplary illustrated timing diagram of FIG. 4, it is illustrated that the timing signal 136 corresponds to the incoming clock signal, therefore the apparatus 102 of FIG. 1 would be considered to the operating at a processing speed relative to a 10% delay.

Based on the timing diagram of FIG. 4, the timing signals 122 and 134 meet the setup time 404 requirement for the second flip flop 146 of FIG. 1. Timing signals 136, 138 and 140 violate the setup time which indicate that the caused delay is too much and therefore the value on the output of the second flip flop 146, output signal 152, may be wrong.

[00034] FIG. 5 illustrates a flow chart representing the steps of a method for determining a processing speed of an integrated circuit. The method begins, step 500, by receiving input signal and an incoming timing signal and a first flip flop to generate a first flip flop output signal, step 502. Similar to the discussion above with regards to FIG. 1, the input signal 106 is received by the first flip flop, flip flop 104, as well as the incoming timing signal 110 such that the first flip flop output signal 114 is generated.

[00035] The next step, step 504, is providing the first flip flop output signal to a delay circuit to generate a delay timing signal. Once again, the first flip flop output signal 114 is provided for the delay 120 as illustrated in FIG. 1 to generate the delay timing signal 122. The delay timing signals are provided to at least one clock speed adjusting circuit such that a plurality of timing adjusted signals are generated, step 506. In the embodiment described above, four speed adjusting circuits are utilized in conjunction with a timing diagram having no clock speed adjustment, such that the signals 122, 134, 136, 138 and 144 are generated. The plurality of timing adjusted signals are thereupon provided to a multiplexer, step 508. The signals 122, 134, 136, 138 and 140 are provided to the multiplexer 132.

[00036] The next step, step 510, is receiving a select delay signal in the multiplexer such that the multiplexer selects one of the plurality of timing adjusted signals to generate a multiplexer output signal. Multiplexer 132 receives the select delay signal 142 to generate the

multiplexer output signal 144. Thereupon, the multiplexer output signal is provided to a second flip flop, step 512. Also, the incoming timing signal is further received by the second flip flop to generate an output timing signal, step 514. The second flip flop 146 receives the incoming timing signal 110 and the multiplexer output signal 144 to generate the output timing signal 152.

[00037] The next step of the method, step 516, includes comparing the output timing signal with a control timing signal. As discussed above with regards to FIG. 3, the control timing signal 316 is compared with the output timing signal 152 using, in one embodiment, a logic gate 318. Thereupon, based on the comparison of the output timing signal 152 relative to the control timing signal 318, the processing speed of the integrated circuit may be determined, thereupon the method is complete, step 518. In another embodiment, further method steps may be performed as indicated by reference block A, 520.

[00038] FIG. 6 illustrates further steps of an alternative method for determining a processing speed of an integrated circuit. The method continues, step 520, relative to the completion of step 516 in the method illustrated in the flow chart of FIG. 5. The next step, step 522, is receiving the input signal from a pseudo-random generator, such as the pseudo-random generator 302 of FIG. 3. The next step, step 524, is receiving the select delay signal from a sequencer, such as the sequencer 304 of FIG. 3.

[00039] Thereupon, the method includes generating a timing result signal based on the comparison of the output timing signal and the control timing signal, step 526. The output timing signal 152 may be compared relative to the control timing signal 316 using the control logic 318 as discussed above with regards to FIG. 3. Thereupon, the timing result signal may be provided to a register, step 528. In one embodiment, the register 320 may store the timing result

signal 324. A determination is made whether more results are required to properly determine the processing speed of the integrated circuit, step 530. In the event more results are requested or required, the method repeats to step 520, receiving another input signal and another select delay signal. When no more results are to be detected, the next step, step 532, is determining the processing speed based on the plurality of timing result signals. Similar to the discussion regarding the timing diagram of FIG. 4, the processing speed is determined based upon, in one embodiment, the delay branches meeting specific set up timing requirements for associated flip flops. Thereupon, the method is complete, step 534.

[00040] FIG. 7 illustrates a method for determining a processing speed of an integrated circuit and utilizing the processing speed determination in conjunction with a binning process for sorting the plurality of integrated circuits. The method begins, step 540, by selecting one of the plurality of integrated circuits, step 542. In one embodiment, the plurality of integrated circuits may now be disposed within a wafer wherein the integrated circuits are etched into the wafer die, prior to cutting of the wafer. In a manufacturing embodiment, the integrated circuit may be selected by placing a control module over a particular integrated circuit on the pre-cut wafer. The next step, step 544, is providing an incoming timing signal to a first flip flop, a first delay module and a second delay module. Similar to the embodiment described above with regards to FIG. 2, the three flop module 200 receives the incoming timing signal. Moreover, the next step includes providing a delay signal to the first delay module and a second delay module, step 546. Once again, as discussed above in one embodiment with regards to FIG. 2, the delay select signal 142 is provided to the three flop module 200.

[00041] The method further includes retrieving a timing output signal from the second delay module, step 548. Based on different embodiments, the timing output signal may be

retrieved directly from the second delay module or may be, in another embodiment, retrieved from the logic gate flip flop 322 as illustrated in FIG. 3. If more results are required to determine the processing speed of the select integrated circuit are required, step 550, the method reverts back to step 542 for re-execution of step 542 through 548. Once the processing speed of the integrated circuit has been determined, the processing speed of the integrated circuit is recorded, step 552. Recording of the processing speed may be performed in any suitable manner to indicate the category or specific processing speed of the selected integrated circuit operates at. For example, in one embodiment, the integrated circuit may be etched with a particular code, such as a bar code, to represent the operating speed. Although any other suitable recording technique, such as recording the speed of the circuit relative to the circuit's location within an external database, may be provided and within the scope of the present invention.

[00042] The next step of the method is determining if there are more integrated circuits on the wafer for the determination of the integrated circuit processing speed. If there are more circuits, step 554, the method once again reverts back to step 542 whereupon steps 542 through 552 are repeated.

[00043] When there are no more integrated circuits for determining the processing speed thereof on the waver, the next step is removing each of the integrated circuits from the central wafer, step 556. Thereupon each of the plurality of integrated circuits may be binned based on the recorded processing speed of each integrated circuit, step 558. Thereupon, the method is complete, step 560. The above method improves the binning process for a wafer having a plurality of integrated circuits disposed thereon. Such that each of the plurality of integrated circuits may be tested for a processing speed and effectively distributed or binned relative to its internal processing speed.

[00044] In one embodiment, the apparatus for determining the processing speed of the integrated circuit requires very little real estate relative to other elements within the integrated circuit. Therefore, based on the reduced size, multiple apparatuses for determining the processing speed may be disposed at various locations throughout the integrated circuit and throughout a wafer containing a plurality of integrated circuits for allowing for the determination of cross sectional measurements of multiple locations to accurately and efficiently determine integrated circuit processing speed without taking up valuable real estate on the integrated circuit dye.

[00045] It should be understood that the implementation of other variations and modifications of the invention and its various aspects will be apparent to those of ordinary skill in the art, and that the invention is not limited by the specific embodiments described herein. For example, module 200 may be modified to include any number of delay modules effectively increasing the reliability of the output signal 152. It is therefore contemplated to cover by the present invention, any and all modifications, variations or equivalents that fall within the spirit and scope of the basic underlying principles disclosed in claim herein.